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IN THE SPECIFICATION

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Please amend the paragraph starting on page 15, line 15 as follows:

-- Once the trench 52 is filled with the isolation oxide 58, the oxide 58 may be patterned such that a shallow cavity 60 is formed along the walls of the channel as indicated in Fig. 4. It should be understood that while the term "cavity" is used to describe the opening formed in the oxide 58, the term is simply used for clarity such that it is easily distinguishable from the trench 52. As can be appreciated, the cavity 60 may also be described as a trench formed in the oxide 58 that extends through the length of the trench 52. In the present exemplary embodiment, the isolation oxide 58 may be etched to form an inverted U-shaped cavity, as illustrated in Fig. 4. In accordance with one exemplary embodiment, each of the plurality of cavities 60 has a depth in the range of approximately 300 angstroms to 1500 angstroms. Further, in accordance with another exemplary embodiment, each cavity 60 may have an aspect ratio of less than or equal to approximately 0.5 to 10. In accordance with another exemplary embodiment, each cavity 60 may have an aspect ratio of less than or equal to approximately 1 to 3. As will be illustrated further below, the exposed edge 62 will form a diode junction[[s]] for the FET 32 having a low junction leakage based on its proximity to the isolation oxide 58. As used herein, the "exposed edge 62" refers to the edge being essentially free of any film, especially oxides and hydrocarbons. --

Please amend the paragraph starting on page 15, line 11 as follows:

-- Once the wordline layers (i.e., oxide 54, polysilicon gate 70 and cap 72) are disposed, the wordlines may be patterned and etched by a conventional means. Next, a nitride layer may be